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EXAMINER	
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ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,507	HO ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-120* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date __.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's communication filed April 7, 2006 in response to PTO office action mailed December 15, 2005. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.

2. In response to the last office action, claims 1, 12, 16, 19, 21-23, 29, 32, 44-46, 51, 55, 58-61, 64, 67, 79-81, 90, 94, 96, 98-100, 106 and 109 have been amended. No claims have been added or canceled. As a result, claims 1-120 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-120 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant argues in remarks on page 63, that the MAC taught by Zaidi is not a switch. Examiner respectfully disagrees with this. As stated in column 23 (referring figs. 20-22), lines 22-29, "Switched channel memory controller" allows multiple DMA (and processors) to simultaneously communicate with multiple output channels. Further in lines 40-45, suggests that CPU bus can be connected to an external flash memory through one channel and SDRAM through another channel. These statements clearly state there are separate communicative interfaces between the connections.

Allowable Subject Matter

5. The indicated allowability of claims 35-38, 39-43, 70-73, 74-78, 112-115, 116-120 is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Specification

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claims 35, 70 and 112 cites the phrase "first and second pages to be overwritten", the first and second pages are not disclosed in specification.

Claim Objections

7. Claim 69 objected to because of the following informalities:

Claim 69 cites "overwriting said first least used page" in line 2. Since claims 67-69 are similar in scope, examiner treated as "overwriting said second least used page" in claim 69.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 22, 32-34, 40, 42-43, 67-69, 75, 77-78, 109-111 and 117-120 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 32-34, 40, 42-43, 67-69, 75, 77-78, 109-111 and 117-120 recites the phrase "at least one internal state of the first central processing unit (CPU)". It is understood from the claim language, the system (method) identifies least recently used (LRU) page, as well as replaces those identified LRU page solely based on internal states of the first CPU, while claims also cites a second CPU also accessing data from line cache. It is not clear how one having ordinary skill in the art would be able to identify and replace pages requested by the second CPU by monitoring internal state of the first CPU?

Claim 22, recites "wherein when said line cache receives said selected one of said first and second address from said line cache arbitration device" in lines 10-11. Claim 22 depends from claim 21, and claim 21 recites an arbitration device translates address and translated addresses are forwarded to cache. It is not clear how cache receives first and second addresses from arbitration device?

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

11. Claim 6 recites the limitation "a second address" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "said second CPU" in lines 25-26. There is insufficient antecedent basis for this limitation in the claim.

Claims 15, 16, 17 and 18 recites the limitation "the CPU" in lines 2, 20, 2 and 2 respectively. There is insufficient antecedent basis for this limitation in the claims.

Claims19, 40 and 117 recites the limitation "said CPU" in lines 16, 4 and 4 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim 51 recites the limitation "said second CPU" in line 20. There is insufficient antecedent basis for this limitation in the claim.

Claims 20 and 97 recites the limitation "4 pages of 8 x 32" in line 2. It is not clear 8 x 32 what? Bits, bytes, lines or blocks?

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

13. Claims 1-11, 13-15, 20, 21-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. As per claims 1, 6, 21, 29 and 32 it is unclear what applicant meant by the phrase "and that generates a first (second) address from said first (second) program read request". Is a line cache interface or CPUs generates an address?

Claims 2-11, 13-15, 20, 22-28, 30-31 and 33-34 are also rejected due to their dependency on rejected claims.

As per claim 40, it is unclear what applicant meant by the phrase "replacement based on usage of said pages". It is not clear what kind of usage applicant meant?

As per claim 1, lines 13-14 cites "a line cache that receives a second address that is based on the first address" and further lines 18-20 cites "when said line cache receives said first address". It is unclear whether cache receives first address as well as a second address based on first address.

As per claim 79, lines 11-12 cites "line cache means for storing and receiving a translated address based on..." and further lines 16-19 cites "said line cache means receives said first address...miss occurs". It is unclear whether cache receives first address as well as a second (translated) address based on first address.

Claims 80-89, 91-93 and 97 are also rejected due their dependency from rejected claim 79.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 11,13-17, 20, 44-48, 50, 52-56, 67-68, 70-71, 73, 79-83, 89, 91-94, and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Zaidi et al. (US 6,601,126 B1) (Zaidi herein after) and Jim Handy (The Cache Memory Book, second edition, published 1998) (Jim herein after submitted as evidentiary reference) and Taylor et al. (5,699,551) (Taylor herein after)

As per claims 1, 44 and 79, Zaidi teaches a cache control system (fig. 1) that controls data flow between a line cache (fig, 1, item 126), a first central processing unit (CPU) (fig. 1, item 110) and first and second memory devices (fig. 1, items 106 and 108), comprising:

a first line cache interface that is associated with the first CPU (taught as cache and channel controller interface the CPU bus, column 4, lines 39-41), that receives a first program read request from CPU and that generates a first address from said first program read request (column 23, lines 30-32);

a first memory interface that communicate with first memory device and second memory interface that communicates with the second memory device (figs. 21-22, two memory devices are connected to memory bus through MAC, which teaches first and second interfaces connected to first and second memory devices);

a cache that receives address that includes memory select portion; and a switch that selectively connects said line cache to one of said first and second memory interfaces (fig. 1, item 126, column 23, lines 31-34 and lines 41-45, taught as CPUs supply a request and an address and address includes both the port, device or memory

bank address and the requested memory location address. Referring figs. 20-22, lines 22-29, "Switched channel memory controller" allows multiple DMA (and processors) to simultaneously communicate with multiple output channels. Further in lines 40-45, suggests that CPU bus can be connected to an external flash memory through one channel and SDRAM through another channel. These statements clearly state there are separate and selective communication interfaces between the connections.).

Zaidi fails to teach line cache receiving first address and comparing address to stored addresses and if match occurs it returns data to CPU, and retrieves data from one of the first and second memories if miss occurs. Zaidi teaches a system with cache memory and it is well known to one of ordinary skill in the art at the time of invention that when CPU issues read request, cache compares the address with the stored addresses and returns the data to CPU and if miss occurs it retrieves data from higher latency storages (see Jim, page 42-43, section 2.1.3) (also applicant's admitted prior art in the background of the invention section).

Zaidi fails to teach sending a second address based on first address. Taylor teaches computer systems using physical cache (receiving translated or second address), virtual memory and translation of address occurring before the cache (cache receiving translated or second address based on first address) (column 1, lines 26-35). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize physical cache as taught by Taylor in the system of Zaidi and Jim because virtual memory provides protection, large address space and physical cache memory are simpler to build (see Taylor column 1, lines 26-40).

As per claims 2-3, 45-46 and 80-81, Zaidi teaches that the first memory device is RAM (fig. 1, item 108).

As per claims 4, 47 and 82, second memory device is flash memory (fig. 1, item 106).

As per claim 5, 48 and 83, first CPU is an advanced risc machine (ARM) processor (column 5, lines 35-36).

As per claims 11, 50 and 89, Zaidi teaches a cache memory as per claim 1 and memories are used for storing data. Zaidi fails to teach cache with a Content Addressable Memory (CAM). Jim teaches a cache memory with CAM, which stores addresses associated with data stored in the cache memory (page 14, sec. 1.5, page 15, fig. 1.7). Jim teaches determining when hit and miss occurs and retrieves data from higher latency memories (first and second memories) when miss occurs (pages 42-43, sec. 2.1.3 and pages 46-47, fig. 2.4). Thus Jim inherently teaches cache state machine.

It would have been obvious to one having ordinary skill in the art at the time of invention have used Zaidi's dual processor system and modified to use the cache with CAM as taught by Jim because CAM permits content of memory to be searched and matched instead of having to specify a memory location in order to retrieve data from memory (page 14, sec. 1.5). This allows data to be stored at any location in a cache (page 16, paragraph 3)

As per claims 13-14, 52-53 and 91-92, Jim teaches a cache replacement algorithm Least Used Page, which replaces least used page with data retrieved form the

first or second memory when miss occurs (page 57, paragraph 2). Thus Jim inherently teaches least used page device.

As per claims 15, 54 and 93, Jim teaches that state transitions of cache state machine are based, in part on at least one internal state of the CPU (page 42, paragraph 2 and 3 and sec. 2.1.3)

As per claims 20 and 97, Jim teaches that cache can have many ways of implementations depending upon the depending upon the address bits used in the system (page 54, paragraphs 2 and 3). Thus Jim inherently teaches cache with 4 pages of 8 x 32.

Claims 16 and 17 are similar in scope with combination of claims 1, 11, 13 and 14. With respect to claim 13-14, Jim teaches least recently used (LRU) cache replacement algorithm and maintains the statistics separately. (See page 57, paragraph 2). The idea behind LRU obviously requires keeping track of what was used and when? This inherently teaches identifying a second least used page (claim 16), and keeping track of LRU inherently suggests that likelihood of LRU page being needed within predetermined period is less and thus replaced (claim 17).

Claims 55-56, 67-68, 70-71, 73, 94 are rejected under same rationales as applied to claims 1-5, 11, 13-14 and 16-17.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-10, 21-28, 30-33, 49, 59-63, 65-66, 84-88, 98-105, and 107-110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi and Jim Handy as applied to claims 1-5, 11, 13-14, 16-17, 44-48 and 79-83 above, and further in view of Barroso et al. (US 6,725,334 B2).

As per claims 6, 49 and 84, Zaidi and Jim teach a dual processor system with two caches (fig. 2, items 202 and 214, first and second processors, and items 208 and 224, two caches). Zaidi and Jim inherently teach cache interface with first and second CPUs and both generates read requests and hence first and second address as taught in claim 1. Zaidi teaches system with two caches for two processors and Zaidi fails to teach cache arbitration device which communicates with first and second cache interfaces and resolves cache access conflicts between first and second CPUs. Barroso teaches a second level cache with switch (fig. 1, item 130 and 120), which provides interfaces with first and second CPU and arbitrates between first and second CPU (column 4, lines 10-21).

It would have been obvious to one having ordinary skill in the art at the time of invention would have modified the multiple cache with multiple processor system of Zaidi and used one cache with switch as taught by Barroso to reduce the cost and the waste of the cache capacity (column 1, lines 45-65).

As per claims 7-8 and 85-86, Zaidi teaches direct interfaces from processors to memory devices (column 22, lines 53-57, taught as p-bus provides access to a cache and m-bus if no cache is needed for access to shared memory).

As per claims 9 and 87, Zaidi and Barroso teach an arbiter and MAC (Zaidi, fig. 2, items 242, 244) and switch (Barroso, fig.1, item 120) to resolve memory access conflict (Zaidi, column 23, lines 40-45).

As per claims 10 and 88, Zaidi teach an application specific integrated circuit (ASIC) which can be used to provide interconnection structure and method for efficient integration variety functional circuits (column 2, lines 63-65). It would have been obvious to one having ordinary skill in the art at the time of invention have used the embedded system of Zaidi to control the hard disk drive and its components for better performance and compact design.

Claims 21-28, 30-31, 59-63, 65-66, 98-105,107-108 are rejected under same rationale as applied to claims 1-5, 11, 13-15, and 6-10 as above.

Claims 32-33 and 109-110 are rejected under same rationales as applied to claims 1-11, 13-14 and 16-17

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19, 58 and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi, Jim Hardy and Barroso as applied to claims 1-10 above, and further in view of Goodsell (US 7,047,387 B2) and Kirovski et al. (Application-Driven Synthesis of Memory-Intensive System-on-Chip).

Claims 19, 58 and 96 are similar in scope with combination of claims 1-11 above. But the combination of Zaidi, Jim, Barroso fails to teach selecting size of the cache based on application running. Goodsell (column 2, lines 20-23 and lines 41-45) and Kirovaski (page 1316, column 2, paragraphs 2 and 5) teach cache size selection based on application. It would have been obvious to one having ordinary skill in the art at the time of the invention to select cache size based on application as taught by Goodsell and Kirovski in the system of Zaidi, Jim and Barroso to balance memory use between processes for better performance (Goodsell, column 2, lines 45-50) and for better (smaller) performance and reduced chip area (see Kirovski, column 2, paragraphs 2 and 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 18, 34, 35-38, 57, 69, 72, 95, 111 and 112-115 rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi, Jim Hardy and Barroso as applied to claims 1-20 above, and further in view of Smith et al. (5,594,886)

As per claim 18, Zaidi, Jim Hardy and Barroso teach all limitations of claims 16-17 as taught above but fail to teach replacing second least used page instead of (first) least used page. Smith teaches replacing second least used page (column 1, lines 59-67). It would have been obvious to one having ordinary skill in the art at the time of the invention to replace second least used page as taught by Smith in system of Zaidi, Jim Hardy and Barroso to improve system performance. As taught by Smith second least used page can be most likely least used page and replacing second least used page improves system performance and it is simple to implement (Smith, column 1, lines 50-67).

Claims 34, 35-38, 57, 69, 72, 95, 111 and 112-115 are similar in combined scope of claims 16-18, as Zaidi, Jim Hardy, Barroso and Smith combined teaches identifying first and second least used pages and replacing one of them.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 12, 29, 39-43, 51, 64-66, 74-78, 90, 106-108 and 116-120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi, Jim Hardy, Barroso and Smith as applied to claims 1-11, 13-20 above, and further in view of Dottling et al. (6,014,756).

As per claim 12, Zaidi, Jim Hardy and Barroso teach all the limitations, but they combined failed to teach accessing one page by one of first and second CPUs, while other of first and second CPUs is accessing another page. Dottling teaches shared cache memory, which allows multiple simultaneous access to data held in different portions (lines or pages) of cache (see Dottling, column 1, lines 38-56). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize shared cache allowing multiple simultaneous access to different portions of cache as taught by Dottling in the system of Zaidi, Jim Hardy, Barroso and Smith to improve system performance (see Dottling, column 1, lines 25-55).

Claims 29, 39, 51, 64, 74, 90, 106 and 116 are also rejected under same rationales as applied to claim 12. Dependent claims 40-43, 65-66, 75-78, 105-108, and 117-120 are in similar scope with respect to claims 16-18 and hence rejected under same rationales as applied to claims 16-18 above.

Conclusion

11. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

6/22/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER